

600V Half-Bridge Driver

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- $I_{\text{O+/- (min)}}$ 130 mA/270 mA
- V_{OUT} 10 V - 20 V
- $t_{\text{on/off (typ.)}}$ 680 ns/180 ns
- **Deadtime (typ.)** 520 ns

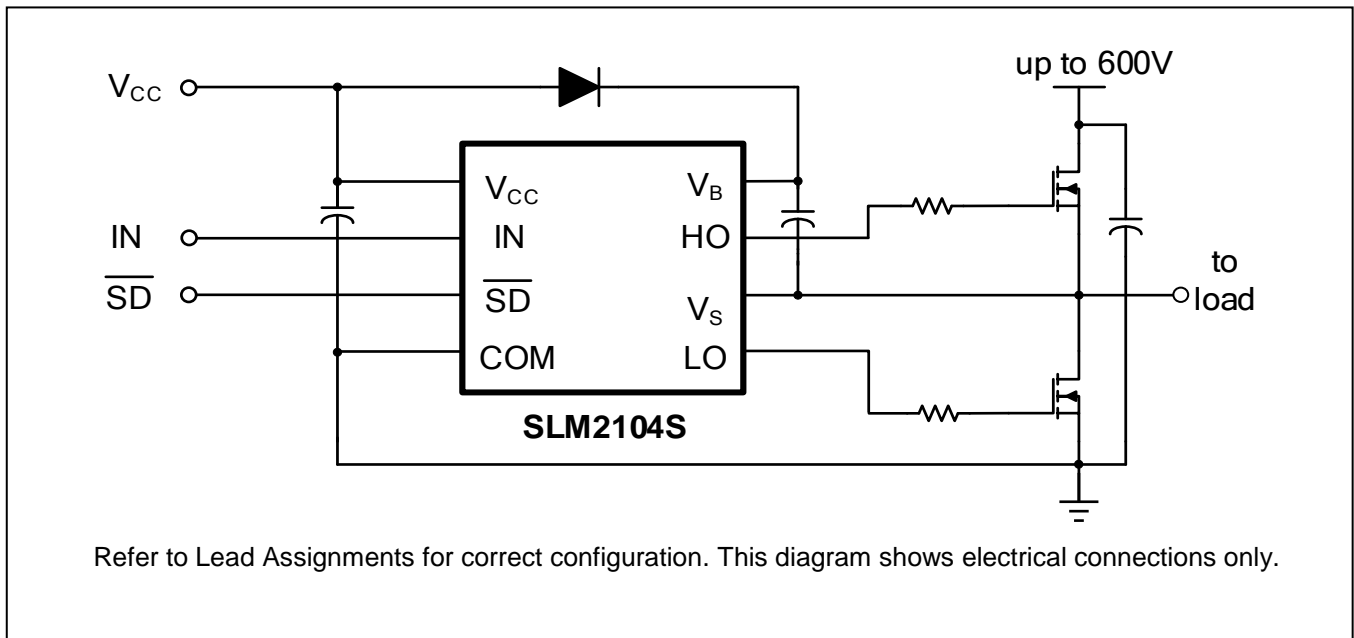
GENERAL DESCRIPTION

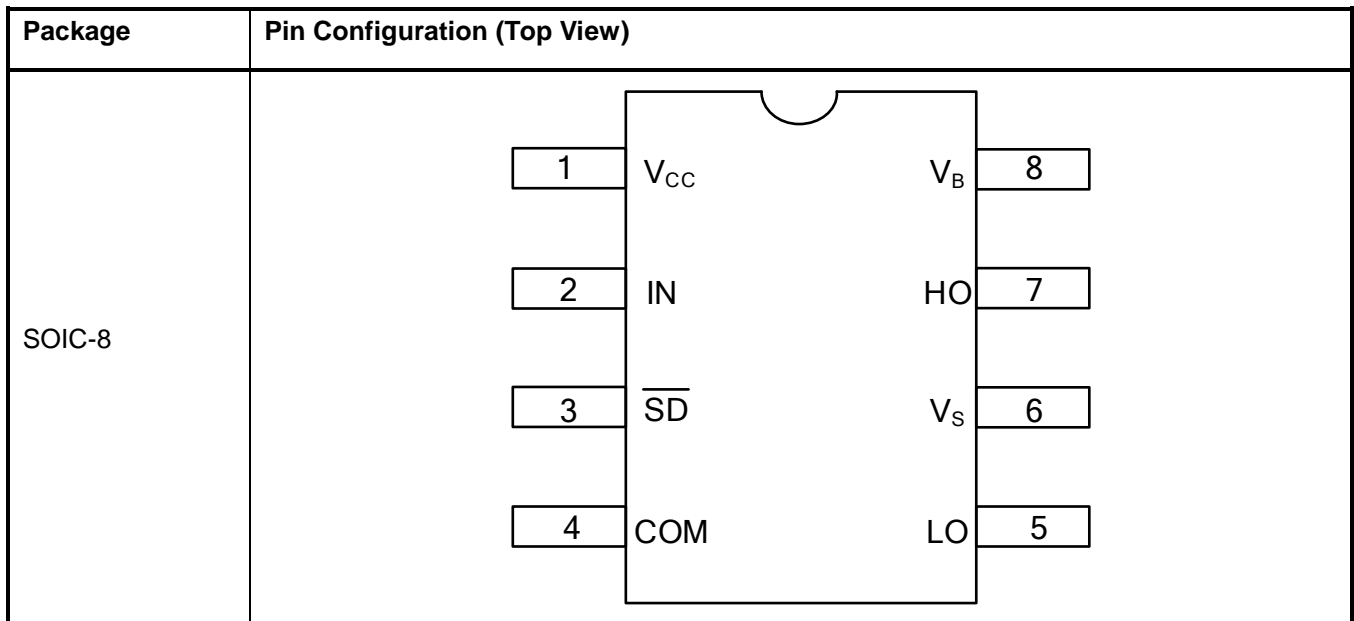
The SLM2104S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOIC-8 package

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

PIN DESCRIPTION

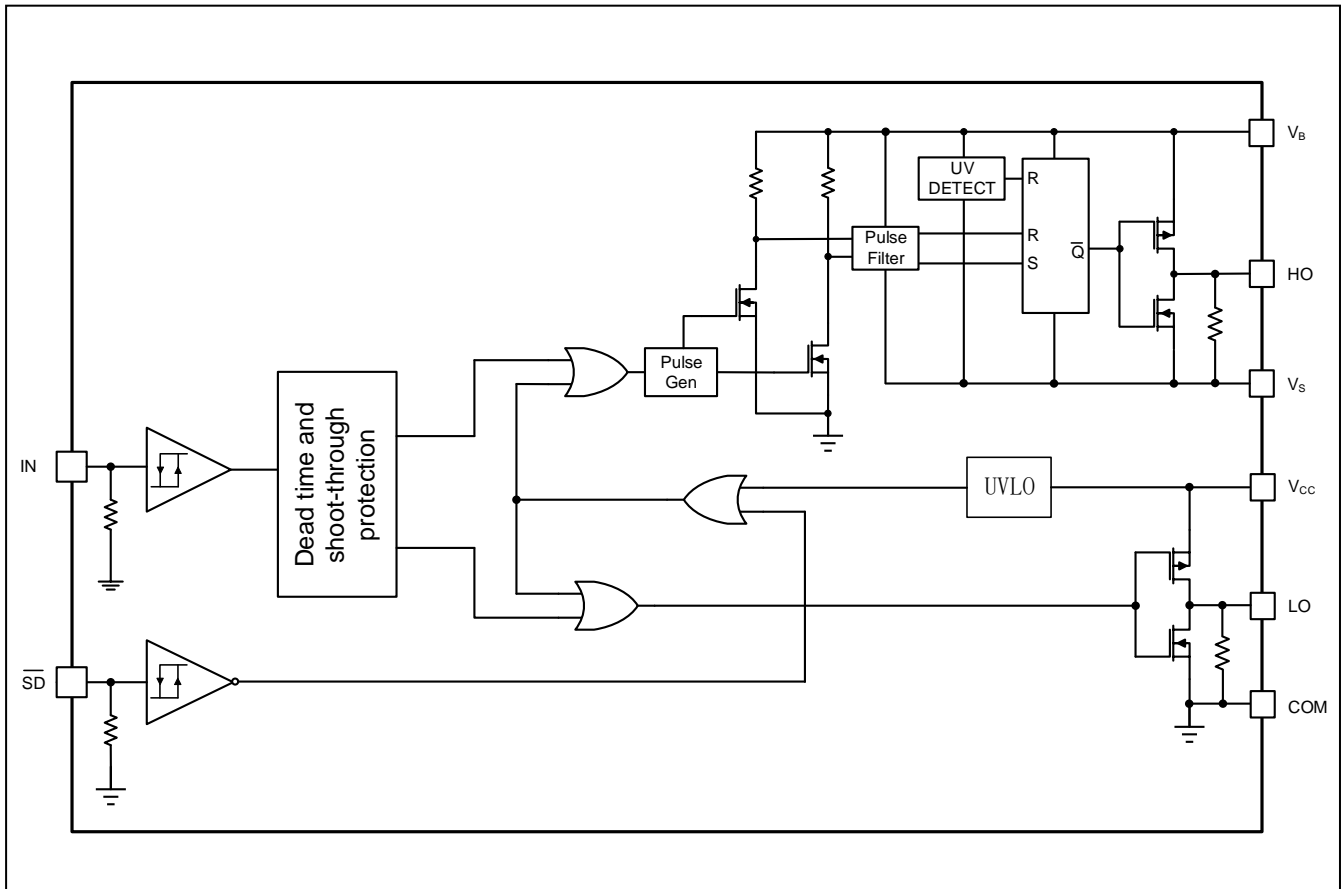
No.	Pin	Description
1	V _{CC}	Low-side and logic fixed supply
2	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
3	$\overline{\text{SD}}$	Logic input for shutdown
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V _S	High-side floating supply return
7	HO	High-side gate drive output
8	V _B	High-side floating supply

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2104SCA-13GTR	SOIC8, Pb-Free	2500/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	-0.3	625	V
V _S	High-side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High-side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V _{LO}	Low-side output voltage	-0.3	V _{CC} + 0.3	
V _{IN}	Logic input voltage (IN & \overline{SD})	-0.3	V _{CC} + 0.3	
dV _S /dt	Allowable offset supply voltage transient	---	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	---	0.625	W
θ _{JA}	Thermal resistance, junction to ambient	---	200	°C/W
T _J	Junction temperature	---	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	V _S + 10	V _S + 20	V
V _S	High-side floating supply offset voltage		600	
V _{HO}	High-side floating output voltage	V _S	V _B	
V _{CC}	Low-side and logic fixed supply voltage	10	20	
V _{LO}	Low-side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage (IN & \overline{SD})	0	V _{CC}	
T _A	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0$ V	---	680	820	ns
t_{off}	Turn-off propagation delay	$V_S = 0$ V	---	180	280	
t_{sd}	Shutdown propagation delay		---	220	300	
t_r	Turn-on rise time		---	70	170	
t_f	Turn-off fall time		---	25	90	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	650	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: IN and \overline{SD} . The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage	$V_{CC} = 10$ V to 20V	2.5	---	---	V
V_{IL}	Logic "0" input voltage		---	---	0.8	
VSD, TH+	SD input positive going threshold		2.5	---	---	
VSD, TH-	SD input negative going threshold		---	---	0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 20$ mA	---	0.45	0.6	
V_{OL}	Low level output voltage, V_O		---	0.15	0.2	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600$ V	---	---	50	μ A
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0$ V	---	60	78	
I_{QCC}	Quiescent V_{CC} supply current		---	220	280	
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5$ V	---	8	15	
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0$ V	---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} supply undervoltage negative going threshold		7.4	8.2	9	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{O+}	Output high short circuit pulsed current	$V_O = 0\text{ V}, V_{IN} = V_{IH}$ $PW \leq 10\ \mu\text{s}$	130	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15\text{ V}, V_{IN} = V_{IL}$ $PW \leq 10\ \mu\text{s}$	270	600		

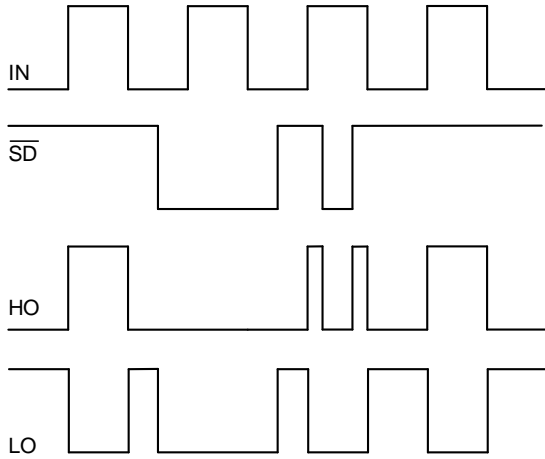


Figure 1. Input/Output Timing Diagram

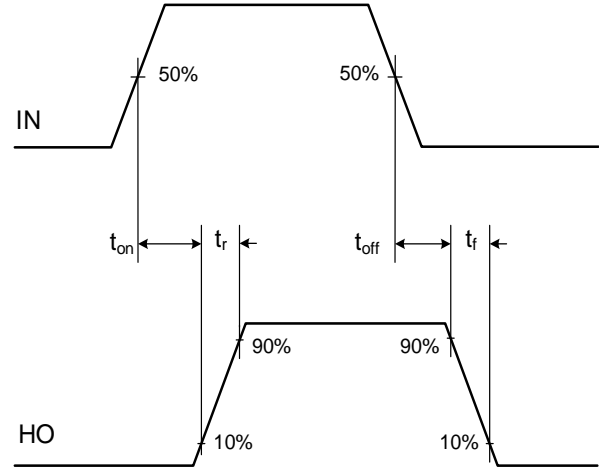


Figure 2. High Side Switching Time Waveform

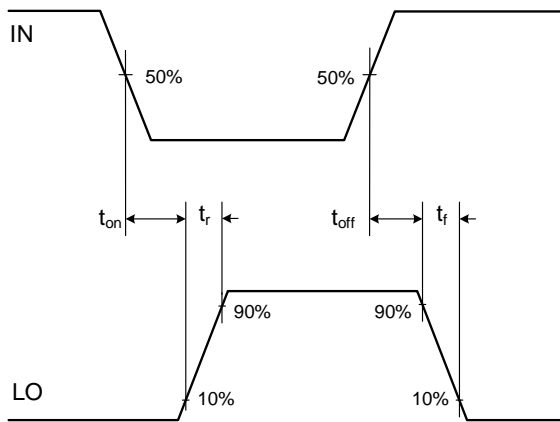


Figure 3. Low Side Switching Time Waveform

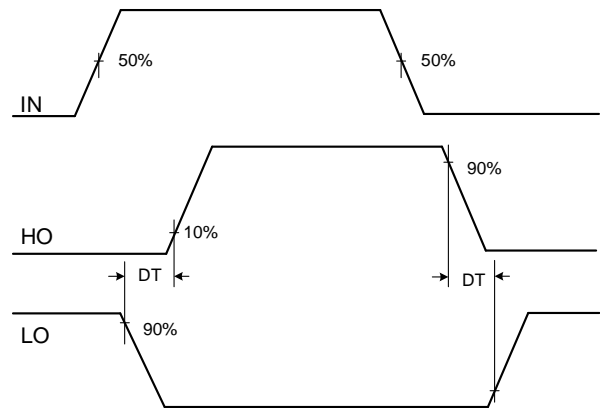


Figure 4. Dead Time Waveform

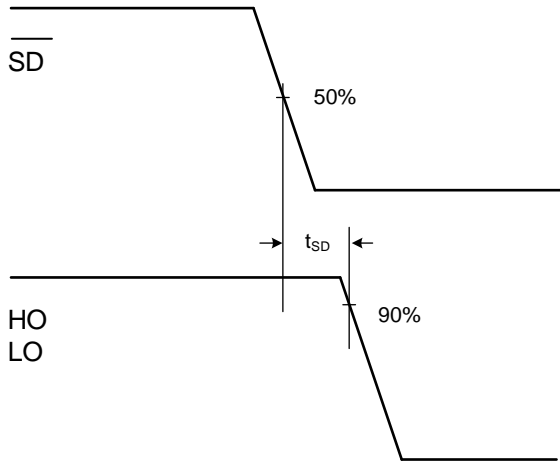


Figure 5. Shutdown Time Waveform

PACKAGE CASE OUTLINES

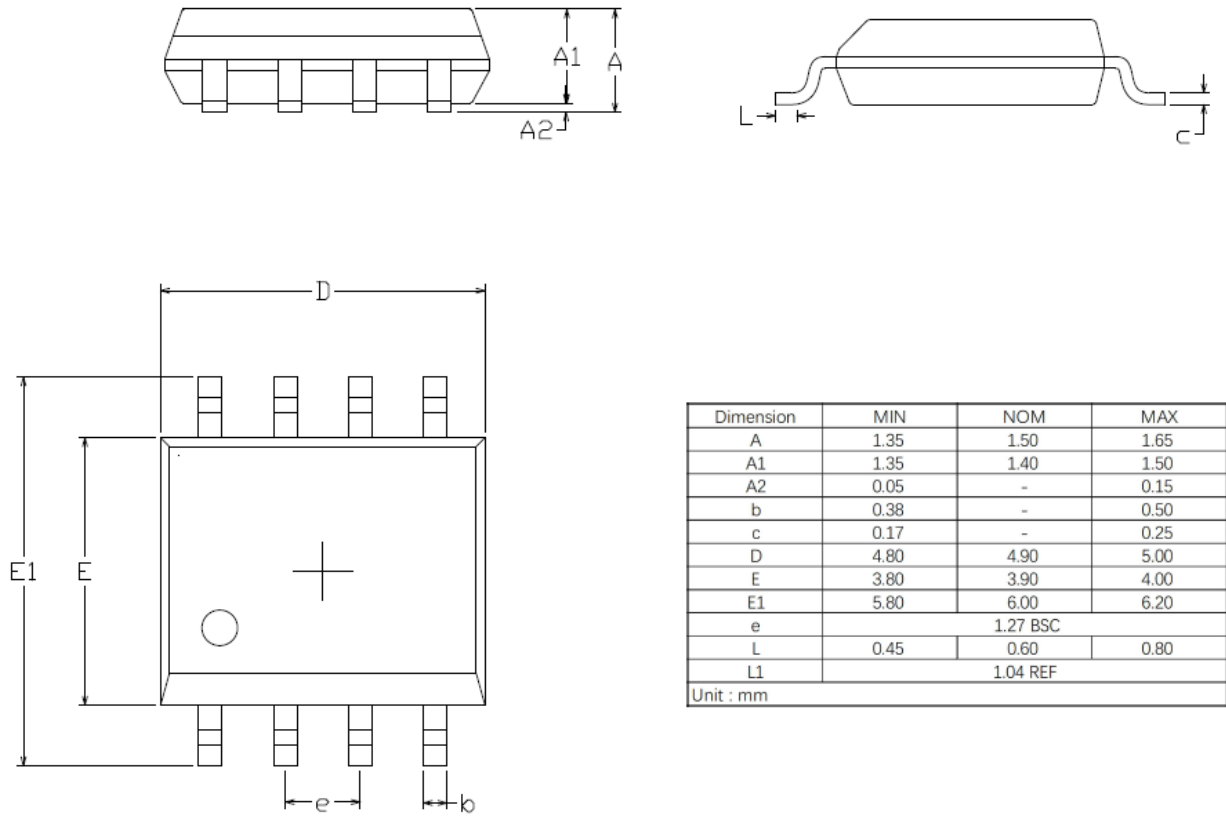


Figure 6. SOIC8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Removed "Figure 1." and "May 2019"
Page 5	Add UVLO threshold for V_{BS} voltage
Rev 1.1 datasheet, 2021-10-29	
Whole datasheet	Update the Logo and format
Page 1	Remove the PDIP package
Page 2	Remove SLM2104SCA-GT and SLM2104SDA-GT in ordering information
Page 5	Update the t_{SD} , t_r and t_{off} in the dynamic electrical characteristics table Update the V_{OH} , V_{OL} , I_{QCC} and I_{IN+} in the static electrical characteristics table